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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,332	01/13/2004	Matthew S. Taubman	50005-172	3464

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EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,332	TAUBMAN, MATTHEW S.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/16/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28 and 30-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28 and 30-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 6/16/2005. Claims 28 and 30-49 are pending and are under examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 28, 30, 31, 35, 38, and 42-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Welland (USP 4,409,500), prior art of record. Figure 3 of Welland shows a circuit having a transistor (24) operating in common base, two input signal pathways (Iin and V_in) coupled to a first terminal (emitter 22) of the transistor, providing a virtual ground at the first terminal of the transistor device (the first terminal of the transistor is at virtual ground because the positive terminal of the differential amplifier is grounded) through a curent path to the virtual ground, wherein the path is continuously uninterrupted at all frequencies, providing an output from the second terminal of the transistor device to a current dependent load (where IRECT is connected to) as called for in claims 28, 35 and 42-43.

Regarding claim 30, controlling the transistor with a servo device (10), providing feedback to the servo device from the first terminal of the transistor.

Regarding claims 31, 38 and 44, the negative feedback is coupled to the negative input of the differential amplifier 10, the positive input of the differential amplifier is coupled to ground.

3. Claims 42-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Dowd et al. (USP 5,123,024), prior art of record. Figure 1 of Dowd et al. shows a circuit having a transistor (14) operating in common base (column 2, lines 54), two input signal pathways (Id at node 5; Idac to node 5) coupled to a first terminal (emitter 16) of the transistor, providing a virtual ground at the first terminal of the transistor device, wherein the virtual ground is provided by a servo device terminal (inverting terminal of the amplifier 8), and wherein no active components (capacitor 12 is a passive component) are positioned between the first terminal of the transistor device and the servo device terminal, electrically coupling a laser device (32) to a second terminal of the transistor device (collector of 14), controlling operation of the laser device with an input signal provided to the first terminal of the transistor device as called for in claims 42 and 44.

4. Regarding claim 43, figure 1 shows two signal input paths.

5. regarding claim 45, figure 4 constant bias current idac, second current source (28).

6. Claim 47 is rejected under 35 U.S.C. 102(b) as being anticipated by Dowd et al. (USP 5,123,024), prior art of record. Figure 1 of Dowd et al. shows transistor device (14), two input signal paths (Idac, Id), low pass filter (15), output (at node 21) to a current dependent load (26) as called for in claim 47.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 33, 34, 36, 40 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welland (USP 4,409,500), prior art of record.

Figure 3 of Welland shows a circuit having a transistor (24) operating in common base, two input signal pathways (Iin and V_in) coupled to a first terminal (emitter 22) of the transistor, providing a virtual ground at the first terminal of the transistor device (the first terminal of the transistor is at virtual ground because the positive terminal of the differential amplifier is grounded) through a curent path to the virtual ground, wherein the path is continuously uninterrupted at all frequencies, providing an output from the second terminal of the transistor device to a current dependent load (where IRECT is connected to).

Welland does not show the current dependent load having a current source providing current to a laser diode as called for in claims 33, 34, 36, 40 and 45. Although Welland does not specifically show the current dependent load that the signal Irect is applied to, one skilled in the art would have been recognized that output current of Welland would be used to drive circuits (loads). The particular type of loads would be dependent upon the environment in which the Welland circuit would have been used. Thus, using a laser diode with a current source as a load would have been an obvious modification of Welland and will not be patentable under 35USC 103(a).

Regarding the constant bias current of claim 34, figure 4 shows the constant bias current (Iin) being applied to the emitter of the transistor 18.

3. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Welland (USP 4,409,500), prior art of record.

Figure 3 of Welland shows a circuit having a transistor (24) operating in common base, two input signal pathways (Iin and V_in) coupled to a first terminal (emitter 22) of the transistor, providing a virtual ground at the first terminal of the transistor device (the first terminal of the transistor is at virtual ground because the positive terminal of the differential amplifier is grounded) through a curent path to the virtual ground, wherein the path is continuously uninterrupted at all frequencies, providing an output from the second terminal of the transistor device to a current dependent load (where IRECT is connected to).

The differences seen between Welland and the present invention is that the present invention calls for the current dependent load to be quantum cascade laser configuration. Although Welland does not specifically show the current dependent load that the signal Irect is applied to, one skilled in the art would have been recognized that output current of Welland would be used to drive circuits (loads). The particular type of loads would be dependent upon the environment in which the Welland circuit would have been used. Thus, using quantum cascade laser diode would have been an obvious modification of Welland and will not be patentable under 35USC 103(a).

4. Claims 32, 39 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welland (USP 4,409,500) in view of Prentice (USP 6,344,762), prior art of record.

Figure 3 of Welland shows a circuit having a transistor (24) operating in common base, two input signal pathways (Iin and V_in) coupled to a first terminal (emitter 22) of the transistor, providing a virtual ground at the first terminal of the transistor device (the first terminal of the

transistor is at virtual ground because the positive terminal of the differential amplifier is grounded) through a curent path to the virtual ground, wherein the path is continuously uninterrupted at all frequencies, providing an output from the second terminal of the transistor device to a current dependent load (where IRECT is connected to).

Figure 4 of Welland does not show a different transistor being coupled to the base of the transistor and the different transistor including ground coupled emitter as called for in claims 32, 39, 46 and 48. Figure 1 of Prentice shows the detailed structures of a differential amplifier having emitter coupled to ground. Prentice's differential amplifier is simply having only two transistors and two resistors thus saving space on a chip and minimize power consumption. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to use Prentice's differential amplifier in place of Welland's differential amplifier (8) for the purpose of saving space and reduce power consumption.

5. Claims 46 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dowd et al. (USP 5,123,024), prior art cited on the PTOL-1449, in view of Prentice (USP 6,344,762), prior art of record. Figure 1 of Dowd et al. shows a circuit having a transistor (14) operating in common base (column 2, lines 54), two input signal pathways (Id at node 5; Idac to node 5) coupled to a first terminal (emitter 16) of the transistor, providing a virtual ground at the first terminal of the transistor device (at high frequency the feedback capacitor 12 is shorted, the first terminal of the transistor is at virtual ground because the positive terminal of the differential amplifier is grounded), providing an output from the second terminal of the transistor device to a current dependent load (30, 32).

Figure 1 of Dowd et al. does not show a different transistor being coupled to the base of the transistor and the different transistor including ground coupled emitter as called for in claim 46. Figure 1 of Prentice shows the detailed structures of a differential amplifier having emitter coupled to ground. Prentice's differential amplifier is simply having only two transistors and two resistors thus saving space on a chip and minimize power consumption. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to use Prentice's differential amplifier in place of Dowd et al.'s differential amplifier (8) for the purpose of saving space and reduce power consumption.

6. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Welland (USP 4,409,500), prior art of record, in view of Dowd et al. (USP 5,123,024).

Figure 3 of Welland shows a circuit having a transistor (24) operating in common base, two input signal pathways (Iin and V_in) coupled to a first terminal (emitter 22) of the transistor, providing a virtual ground at the first terminal of the transistor device (the first terminal of the transistor is at virtual ground because the positive terminal of the differential amplifier is grounded) through a curent path to the virtual ground, wherein the path is continuously uninterrupted at all frequencies, providing an output from the second terminal of the transistor device to a current dependent load (where IRECT is connected to).

Figure 3 of Welland does not show a low pass filter coupled to the base of the transistor device as called for in claim 49. Figure 1 of Dowd et al. show a low pass filter (capacitor 15) coupled to the base of the transistor device (14) for the purpose of filtering out the noise components. Therefore, it would have been obvious to a person skilled in the art at the time the

invention was made to include a low pass filter at the base of the transistor device of Welland for the purpose of filtering out noise thus preventing erroneous operation.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

7/12/2005